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A Novel Small-Signal Knowledge-Based Neural Network Modeling Approach for Packaged Transistors

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Abstract : This paper proposes a novel small-signal knowledge-based neural network modeling method for packaged transistors. Separate neural networks are proposed to represent the behaviors of packages covering the core transistor. An advanced training method is developed by utilizing the different parameters to adjust the different characteristics of the packaged transistors, which avoid parameter adjustment repeatedly and speed up the modeling process. The proposed model combing the neural networks with the core transistor model is trained to present the entire small-signal behavior of the packaged transistors. Measurement data of the radio frequency (RF) power laterally diffused metal-oxide semiconductor (LDMOS) transistor are used as the application example to verify the capability of the proposed method. The results demonstrate that the proposed model is more accurate than existing models.

Keywords - small-signal model, transistors, neural network, modeling.

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I. Introduction

With the development of electronic technology, the accurate computer-aided design (CAD) models of packaged transistors play a decisive role in the circuit/system design [1, 2]. The equivalent-circuit-based model [3] and Electromagnetic (EM) - based model [4] are good for modeling mature technologies and existing transistors. However, with the increasing design complexities and shorter design cycles, the conventional CAD approaches are difficult to satisfy the requirements of precision and speed at the same time. New semiconductor technologies and materials continue to evolve making it necessary to develop efficient modeling algorithms for packaged transistors.

Recently, Knowledge-based neural network modeling techniques have been recognized as useful alternatives to conventional technologies in microwave modeling [5-7]. The knowledge-based model exploit existing knowledge in the form of empirical or equivalent circuit models together with neural networks to develop a more accurate model. The evaluation from input to output of a knowledge-based model is also very fast. Knowledge-based techniques have been utilized in transistors modeling when the mathematical model is not available [8]. However, the existing knowledge-based neural network methods for transistors modeling mainly focus on the core transistor without modeling the package circuit [9, 10]. Systematic and fast modeling methods for packaged transistors are still an open research topic.

In this paper, a novel small-signal modeling method using knowledge-based neural networks for packaged transistors is proposed. Separate neural networks are adopted to represent the nonlinear relationship between the frequency and the ***S***-parameters. An advanced training method is proposed for the model development. The proposed model can match the device well and exceed the current capabilities of existing device models.

II. Proposed Modeling Method for Packaged Transistors

Packages of transistors typically contain a metal flange and a dielectric window frame. The core transistor is bonded to the die-bond area inside the cavity of the window frame. Metal leads are provided at the input and output sides of the window frame to allow for connection to external circuitry. Based on the physical structure of the packaged transistor, we propose to divide the total structure into three parts: the input package circuit, the core transistor circuit and the output package circuit, and create the CAD modules for these three parts respectively.

2.1. Proposed DC model

In general, the packaged circuit is composed of linear devices, which does not affect the DC characteristics of the device. The DC characteristics of the device are affected only by the core circuit. In this

paper, we proposed to use the modeling method in literature [9] to create the core circuit model. We define the knowledge model in this paper to represent the existing transistor model. Because the DC characteristics of the existing transistor model and that of the core circuit are not the same, we propose to establish a mapping network to map the inputs of the knowledge model onto the core circuit. Because the mapping network is nonlinear and unknown, neural networks (ANN_1) are proposed to be use as the mapping network. The proposed DC model contains the knowledge model and the input mapping network, shown in Fig.1. After training the neural networks, the proposed DC model can represent the behaviors of the core circuit. Let $V_s^c = [V_{gs}^c, V_{ds}^c]^T$ and $I_s^c = [I_{gs}^c, I_{ds}^c]^T$ represent the voltage and current signals of the knowledge model respectively. Let $V_s^f = [V_{gs}^f, V_{ds}^f]^T$ and $I_s^f = [I_{gs}^f, I_{ds}^f]^T$ represent the voltage and current signals of the core circuit respectively. The proposed DC model exceeds the knowledge model current capabilities by adding more free variables. When the knowledge model operates with the signals (V_{gs}^c, V_{ds}^c) instead of the signals (V_{gs}^f, V_{ds}^f), the output current of the knowledge model I_{ds}^c can match that of the modeled device I_{ds}^f accurately. The neural network is used to describe the nonlinear relationship between the signals of the knowledge model (V_{gs}^c, V_{ds}^c) and the signals of the modeled device (V_{gs}^f, V_{ds}^f) as

$$(V_{gs}^c, V_{ds}^c) = f_{ANN}(V_{gs}^f, V_{ds}^f, \mathbf{w}_1) \tag{1}$$

where f_{ANN} represents a multilayer feedforward neural network, and $\mathbf{w}_1$ is a vector containing all internal synaptic weights in the neural network f_{ANN}.

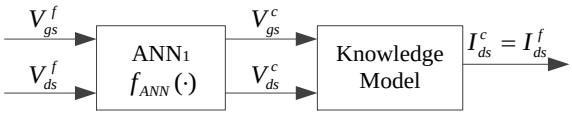

Figure.1 DC model structure.

2.2. Proposed S-parameters model structure

In the packaged transistors, both the core circuit and the package circuits affect the small-signal characteristics of the device. When the core circuit and the package circuits are modeled in terms of their scattering parameters, scattering-matrix analysis can be applicable to small-signal modeling of the packaged transistor. We proposed to create the small signal model for the input package circuit, the core circuit and the output package circuit respectively, and calculate the ***S***-parameters for the model device. The structure of the proposed small signal model is shown in Figure 2. The core module consist of the knowledge model and a neural network ANN_1 represent the small-signal characteristics of the core circuit. The core module can ensure the DC as well as the ***S***-parameters characteristics. Two neural networks are proposed to represent the behaviors of the input and output package circuits respectively. The packaged module can be achieved only using the terminal signals, instead of the internal and physical structure information of the transistor. The ***S***-matrix module based on the literature [5] is constructed realizing the calculation of ***S***-parameters between the packaged transistor and its three parts.

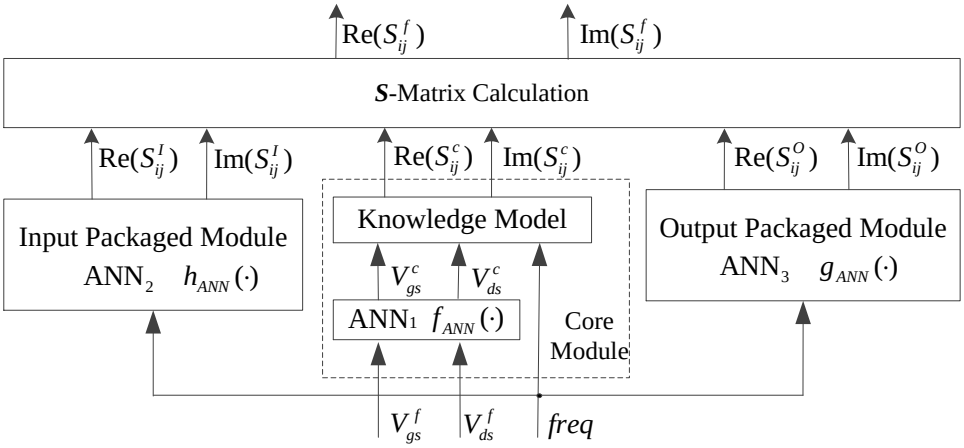

Figure.2 Proposed small-signal model structure.

In Figure 2, the modules ANN_2 and ANN_3 respectively represent the performance of the input/output package circuits which consist of passive components such as bond wires, MOS capacitors and so on. Because the input/output package circuit consists of linear components, the unique input of the packaged modules is the frequency. The output signals of the ANN_2 $\mathrm{Re}(S_{ij}^I)$ and $\mathrm{Im}(S_{ij}^I)$ are the real and imaginary parts of S_{11}, S_{12} and S_{22} of the input packaged circuit. Similarly, $\mathrm{Re}(S_{ij}^O)$ and $\mathrm{Im}(S_{ij}^O)$ are the output signals of the output package circuit respected by the ANN_3. For the core module, bias voltages and frequency are the input signals, and the real and imaginary parts of ***S***-parameters $\mathrm{Re}(S_{ij}^c)$ and $\mathrm{Im}(S_{ij}^c)$ are the output signals. The ***S***-parameters of the modeled device $\mathrm{Re}(S_{ij}^f)$ and $\mathrm{Im}(S_{ij}^f)$ can be calculated with ***S***-matrix calculation module. In the proposed model, the packaged modules represent the nonlinear relationship between the frequency and the ***S***-parameters, which can be described as

$$(\mathrm{Re}(S_{ij}^I), \mathrm{Im}(S_{ij}^I)) = h_{ANN}(freq, \mathbf{w}_2) \tag{2}$$

$$(\mathrm{Re}(S_{ij}^O), \mathrm{Im}(S_{ij}^O)) = g_{ANN}(freq, \mathbf{w}_3) \tag{3}$$

where h_{ANN} and g_{ANN} represents multilayer feedforward neural network, and $\mathbf{w}_2$ and $\mathbf{w}_3$ are vectors containing all internal synaptic weights in the neural network h_{ANN} and g_{ANN} respectively.

Usually, the mathematical relationship between the frequency and the ***S***-parameters of the packaged circuit is not available. When more bond wires, MOS capacitors and integrated capacitor are added into the package circuit to ease external matching-circuit design, the relationship between the frequency and the ***S***-parameters is more complicated. The proposed small-signal model with high precision and high speed can be achieved only using the terminal signals, instead of the internal and physical structure information of the transistor. To make the proposed knowledge-based neural network model represent the DC and small-signal characteristics of the actual device, we propose a new training method in the next subsection.

2.3. Proposed training method

A knowledge-based neural network model cannot represent the packaged transistor accurately until it learns the related data. Therefore, the neural network training is an important step during the model development. The training process automatically adjusts the weights in the neural network so that the output of the model can fit the device data accurately. The training error represents the difference between the device data and the model. Equation (4) and (5) represent the training error of DC, and ***S***-parameters characteristics, respectively:

$$E(\boldsymbol{w}) = \frac{1}{2}\sum_{n=1}^{N} \| I(V_{gs}^{f,n}, V_{df}^{f,n}, \boldsymbol{w}_1) - I_D^n \|^2 \tag{4}$$

$$E(\boldsymbol{w}) = \frac{1}{2}\sum_{n=1}^{N} \| S(V_{gs}^{f,n}, V_{ds}^{f,n}, freq^n, \mathbf{w}_2, \mathbf{w}_3) - \boldsymbol{S}_D^n \|^2 \tag{5}$$

where $\boldsymbol{I}_D$ and $\boldsymbol{I}(.)$ represent the DC responses of the packaged transistor data and the proposed model, respectively. The superscript *n* represents the training data index, and *N* represents the total number of the training data. $\boldsymbol{S}_D$ and $\boldsymbol{S}(.)$ represent the ***S***-parameters of the packaged transistor data and the proposed model, respectively.

In order to improve the modeling efficiency, we propose a four-stage training method. In the first stage, we initialize the weight value of the ANNs avoiding the proposed model degrading the knowledge model performance. In the second stage, we adjust the weight $\mathbf{w}_1$ of the neural network in Figure 1 making the DC model match the device data in the DC simulation. In the third stage, we adjust the weights $\mathbf{w}_2$ and $\mathbf{w}_3$ of the neural networks in Figure 2 making the proposed small-signal model match the device data in the ***S***-parameters simulation. In the fourth stage, we train the proposed overall model by simultaneously train the DC model and the small-signal model again to finally achieve the modeling accuracy. The proposed method controls the DC and small-signal performance of the model with different weight parameters, which reduce the mutual interference of the optimized parameters and avoid changing the optimized parameters repeatedly. After training, the proposed model can be more accurate than the existing model, and it can replace the actual device to plug into an original circuit for design and simulation. The details of the steps for the proposed training process are shown as follows:

Step 1) Initialize the ANN_1 by solving $V_{gs}^c = V_{gs}^f$ and $V_{ds}^c = V_{ds}^f$, and obtain the initial variables $\boldsymbol{w}_1^0$. Initialize the ANN_2 by solving $\mathrm{Re}(S_{12}^I) = \mathrm{Re}(S_{21}^I) = 1$ and other **S**-parameters equals 0, and obtain the initial

variables $\boldsymbol{w}_2^0$. Initialize the ANN_3 by solving $\text{Re}(S_{12}^o)=\text{Re}(S_{21}^o)=1$ and other **S**-parameters equals 0, and obtain the initial variables $\boldsymbol{w}_3^0$. This step can avoid degrading the knowledge model performance.

Step 2) Adjust the weight $\boldsymbol{w}_1^0$ to $\boldsymbol{w}_1^*$ by solving the equation (4) and obtain the bias voltage of the knowledge model V_{gs}^c and V_{ds}^c, which make the proposed model match the device data in the DC simulation.

Step 3) Adjust the weights $\boldsymbol{w}_2^0$ to $\boldsymbol{w}_2^*$ and $\boldsymbol{w}_3^0$ to $\boldsymbol{w}_3^*$ by solving the equation (5) and obtain the $\text{Re}(S_{ij}^I)/\text{Im}(S_{ij}^I)$ and $\text{Re}(S_{ij}^O)/\text{Im}(S_{ij}^O)$, which make the proposed small-signal model match the device data in the ***S***-parameter simulation.

Step 4) Fine tune the weights $(\boldsymbol{w}_1^*,\boldsymbol{w}_2^*,\boldsymbol{w}_3^*)$ to $(\boldsymbol{w}_1^\#,\boldsymbol{w}_2^\#,\boldsymbol{w}_3^\#)$ making the training error as small as possible, which can improve the performance of the proposed model further.

III. Experimental Verification

In this experiment, measured data of the laterally diffused metal-oxide semiconductor (LDMOS) packaged transistor AFT18S230 are used as the training data and test data. The range of them used in this example is showed in Table 1. The LDMOS transistor AFT18S290 model in Advanced Design System (ADS) is used as the knowledge model. The mismatch between the knowledge model and the measured data cannot be ignored. The proposed model is trained using the proposed four-stage training method which has been introduced in section 2.3. The proposed model learns the training data by automatically adjusting the weight of the neural networks. Test data which are different with the training data are used to validate the accuracy of the constructed model. Table 2 gives the test error of the knowledge model and the proposed model. This result demonstrates that the proposed method improves the current capabilities of the knowledge model. In order to further show the detailed results, the I-V and ***S***-parameters comparison between the measured data and the models are shown in Fig.3 and Fig.4, respectively. Good agreements between the proposed model and the measured data can be observed.

Table.1 Training data and test data for DC and ***S***-parameters modeling.

		V_{gs} (V)	V_{ds} (V)	*freq* (GHz)
DC Simulation	Training Data	2.55:0.1:3.25	-0.5:1:32.5	
	Test Data	2.6:0.1:3.2	0:1:32	
***S*-Parameters Simulation**	Training Data	1.35:0.1:1.45 2.68:0.05:2.78	26.5:1:29.5	1.7:0.05:3.1
	Test Data	1.4,2.7,2.75	28	1.7:0.05:3.1

Table.2 Test error of the models for DC and ***S***-parameters simulation.

Error (%)	I_{ds}	$\text{Re}(S_{11})$	$\text{Im}(S_{11})$	$\text{Re}(S_{12})$	$\text{Im}(S_{12})$	$\text{Re}(S_{21})$	$\text{Im}(S_{21})$	$\text{Re}(S_{22})$	$\text{Im}(S_{22})$
Knowledge Model	6.7	6.8	8.1	12.3	12.6	8.2	9.5	28.6	31.9
Proposed Model	0.6	0.9	1.2	3.5	3.4	1.7	1.5	1.9	1.2

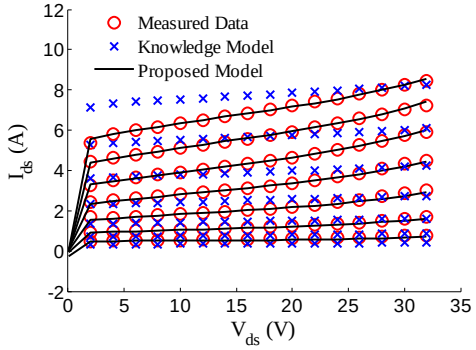

Figure.3 I-V comparison between the measured data and the models for the LDMOS transistor.

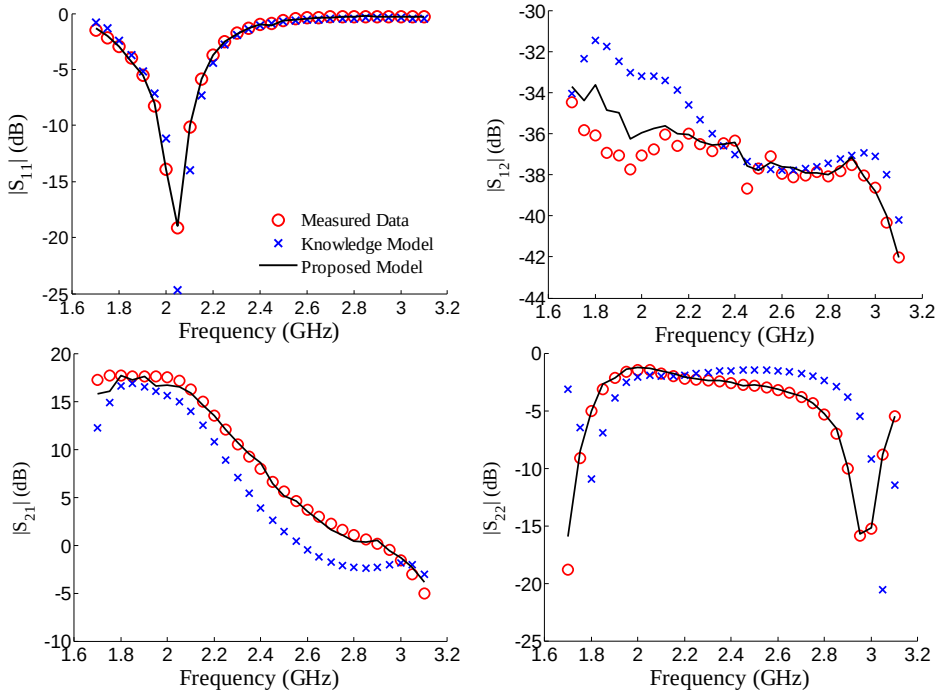

Figure.4 Comparison of ***S***-parameters between the measured data and the models for the LDMOS transistor at the typical work bias point ($V_{gs} = 2.75V, V_{ds} = 28V$).

In this example, the proposed model are operated in hamonic balance (HB) simulation to further verify the effectiveness of the advanced modeling methodology. The models work at the fundamental frequency $1.805GHz$, the source impedance $1.535 - j4.232\Omega$, the load impedance $1.403 - j3.748\Omega$, the bias voltage $(2.75V, 28V)$ and the different input powers (P_{in}: from 4.5 to 16.5dBm, step 2dBm). The comparison results of the gain and the power added efficiency (PAE) between the measured data and the models are shown in Fig.5, demonstrating that the HB respons of the proposed model is much closer to the measured data than that of the knowledge model. This result provides a good foundation for the large signals modeling in the future work.

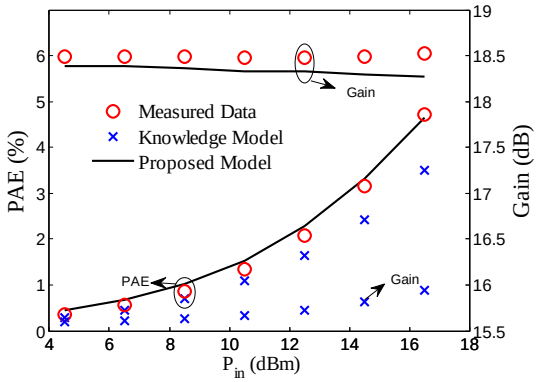

Figure.5 Comparison of the gain and PAE between the measured data and the models for the LDMOS transistor.

IV. Conclusions

In this paper, the novel model combing the separate neural networks with the core transistor model is proposed to present the entire small-signal behavior of the packaged transistors for the first time. The advanced training method can find the appropriate parameters efficiently, and the trained model can represent the linear characteristic of the practical device accurately. The proposed model is achieved only using the terminal signals, instead of the internal and physical structure information of the packaged transistor. This advantage makes the novel method suitable for more and more complex devices meeting the demand of modern technology development.

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